IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Feng-Jong Edward Yang et al.	)	Group Art Unit: 2155
	)	
Application No.: 09/650,195	)	Examiner: K. Bates
	)	
Filed: August 29, 2000	)	
	)	
For: METHOD AND APPARATUS FOR ACCESSING EXTERNAL MEMORIES	)	

TRANSMITTAL FOR APPEAL BRIEF

U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Appeal Brief-Patents
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

Transmitted herewith is an Appeal Brief in support of the Notice of Appeal filed February 2, 2006.

A credit card payment form for ☐ $250.00 ☒ $500.00 to cover the Government fee.

The Commissioner is hereby authorized to charge any other appropriate fees that may be required by this paper that are not accounted for above, and to credit any overpayment, to Deposit Account No. 50-1070.

Respectfully submitted,

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Date: April 3, 2006

PATENT
Attorney Docket No. F0255

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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APPEAL BRIEF

U.S. Patent and Trademark Office
Customer Window, Mail Stop Appeal Brief – Patents
Randolph Building
401 Dulany Street
Alexandria, Virginia 22314

Sir:

This Appeal Brief is submitted in response to the rejection mailed November 2, 2005 and in support of the Notice of Appeal filed February 2, 2006.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Advanced Micro Devices, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals, interferences or judicial proceedings.

III. STATUS OF CLAIMS

Claims 1-5, 7, 9-13, 15-19 and 21-23 are pending in this application. All of the pending claims are the subject of the present appeal.

IV. STATUS OF AMENDMENTS

No Amendment has been filed subsequent to the Office Action mailed November 2, 2005.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Each of the independent claims involved in this appeal is recited below, followed in parenthesis by examples of where support can be found in the specification and drawings for the claimed subject matter. In addition, each dependent claim argued separately below is also summarized in a similar manner.

Claim 1 recites: A network device configured to control communication of data frames between stations (page 3, line 30 to page 4, line 8, Fig. 1, 110), comprising: a plurality of receive devices corresponding to ports on the network device, the receive devices configured to receive data frames from the stations (page 4, lines 9-21, Fig. 1, 120 and 130); and an external memory interface (Fig. 2, 140) configured to: receive data from the plurality of receive devices (page 5, lines 8-10, Fig. 2, 120 and 130), transfer a portion of the data received from a first group of the receive devices (Fig. 2, 120) to a first memory (Fig. 2, 150) and a second memory (Fig. 2, 160) in an alternating manner (page 7, lines 1-10), and transfer a portion of the data received from a

second group of the receive devices (Fig. 2, 130) to the first memory and the second memory in an alternating manner (page 7, lines 1-10), generate odd address information when transferring data via a first external memory bus to the first memory (page 6, last paragraph), and generate even address information when transferring data via a second external memory bus to the second memory (page 6, last paragraph).

Claim 2 recites: The network device of claim 1, wherein the external memory interface includes: a scheduler coupled to the receive devices and configured to enable the received data frames to be output to the first and second memories (Fig. 2, 230), the scheduler simultaneously outputting first and second selection signals for outputting data from one of the first group of receive devices and one of the second group of receive devices, respectively (page 6, lines 9-16).

Claim 4 recites: The network device of claim 1, wherein the external memory interface is further configured to simultaneously transfer the portions of the data from the first and second groups of receive devices to the first and second memories (page 6, lines 17-21).

Claim 7 recites: The network device of claim 5, wherein the first and second external memory buses are each 8-bytes wide and operate at a frequency of 100 MHz (page 8, lines 27-30).

Claim 10 recites: In a network device that controls communication of data frames between stations, a method of storing data frame information, comprising: receiving a plurality of

data frames (page 5, lines 25-26, Fig. 3, 310); temporarily storing the received data frames in a plurality of receive devices (page 5, lines 26-28, Fig. 3, 320); and simultaneously transferring data frame information to at least a first memory and a second memory (page 6, lines 17-21, Fig. 3, 350), wherein the simultaneously transferring includes: alternating the transferring of data frame information from a first group of the receive devices to the first and second memories, and alternating the transferring of data frame information from a second group of the receive devices to the first and second memories, wherein when data frame information from the second group of receive devices is being transferred to one of the first and second memories, data frame information from the first group of receive devices is being transferred to the other of the first and second memories (page 7, lines 1-10, page 8, lines 8-14, Fig. 3, 360 and Fig. 5).

Claim 11 recites: The method of claim 10, further comprising: simultaneously transmitting selection signals to first and second receive devices for selectively outputting data stored in the first and second receive devices (page 6, lines 9-16, Fig. 3, 330).

Claim 16 recites: A data communication system for controlling the communication of data frames between stations, comprising: a plurality of receive devices configured to receive data frames from the stations (page 4, lines 9-21, Fig. 1, 120 and 130); a scheduler coupled to the plurality of receive devices and configured to generate selection signals to selectively output data frame information from the receive devices (page 5, lines 13-22, Fig. 2, 230); a switching device configured to: receive the data frame information, and simultaneously transfer data frame information from one of a first group of receive devices via a first external memory bus and data

frame information from one of a second group of receive devices via a second external memory bus (page 6, lines 17-21, Fig. 2, 240); a first memory (Fig. 2, 150) configured to receive data frame information from the first external memory bus (Fig. 2, 170); and a second memory (Fig. 2, 160) configured to receive data frame information from the second external memory bus (Fig. 2, 180), wherein the switching device is further configured to: generate data address information having odd addresses for data transferred to the first memory, generate data address information having even addresses for data transferred to the second memory (page 6, last paragraph), transfer data frame information from the first group of receive devices to the first and second external memory buses in an alternating manner, and transfer data frame information from the second group of receive devices to the first and second external memory buses in an alternating manner (page 7, lines 1-10, page 8, lines 8-14, Fig. 3, 360 and Fig. 5).

Claim 17 recites: The system of claim 16, further comprising: first and second multiplexers (Fig. 2, 210 and 220) coupled to the first and second groups of the receive devices, respectively, each of the first and second multiplexers being configured to receive the selection signals from the scheduler and to output a portion of a data frame (page 6, lines 9-16).

Claim 18 recites: The system of claim 17, wherein the switching device is further configured to transfer data received from the first multiplexer to the first and second external memory buses in an alternating manner and to transfer data received from the second multiplexer to the first and second external memory buses in an alternating manner (page 7, lines 1-10, page 8, lines 8-14, Fig. 3, 360 and Fig. 5).

Claim 21 recites: The network device of claim 1, wherein the external memory interface is further configured to: transfer data from one of the first group of receive devices to the first memory during a first clock cycle, transfer data from one of the second group of receive devices to the second memory during the first clock, transfer data from one of the first group of receive devices to the second memory during a second clock cycle, the second clock cycle immediately succeeding the first clock cycle, and transfer data from one of the second group of receive devices to the first memory during the second clock cycle (page 7, lines 1-10).

Claim 23 recites: The system of claim 16, wherein the switching device is further configured to: alternate the transfer of data frame information from the first group of receive devices to the first and second external memory buses each clock cycle, and alternate the transfer of data frame information from the second group of receive devices to the first and second external memory buses each clock cycle (page 7, lines 1-10).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 10, 11, 13, 15 and 22 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Humphrey et al. (U.S. Patent No. 4,933,846; hereinafter Humphrey).

B. Claims 1-5, 9, 12, 16-19, 21 and 23 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Humphrey in view of Mann (U.S. Patent No. 6,021,477).

C. Claim 7 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Humphrey in view of Mann and further in view of Runaldue et al. (U.S. Patent No. 6,052,751; hereinafter Runaldue).

VII. ARGUMENT

A. Rejection under 35 U.S.C. § 102 based on Humphrey

1. Claims 10, 13, 15 and 22

The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention always rests upon the Examiner. In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). A proper rejection under 35 U.S.C. § 102 requires that a single reference teaches every element set forth in the claim, either expressly or inherently. See M.P.E.P. § 2131.

With these principles in mind, claim 10 recites a method of storing data frame information in a network device that controls communication of data frames between stations that includes receiving a plurality of data frames. The method includes simultaneously transferring data frame information to at least a first memory and a second memory, wherein the simultaneously transferring includes: alternating the transferring of data frame information from a first group of the receive devices to the first and second memories, and alternating the transferring of data frame information from a second group of the receive devices to the first and second memories, wherein when data frame information from the second group of receive devices is being transferred to one of the first and second memories, data frame information from the first group of receive devices is being transferred to the other of the first and second memories. The Office Action states that Humphrey discloses these features and points to col. 3, lines 1-16, col. 5, lines 55-63, col. 7, lines 58-61 and col. 8, lines 57-62 for support (Office Action – page 3). Appellants respectfully disagree.

Humphrey at col. 3, lines 1-16 discloses interleaved memory banks to which a plurality of processors may be individually coupled via first and second common buses which are selectively

connectable on an alternating basis to the first and second memory banks to allow addresses and data to be transferred therebetween. This portion of Humphrey does not disclose alternating the transferring of data frame information from a first group of the receive devices to the first and second memories, and alternating the transferring of data frame information from a second group of the receive devices to the first and second memories. This portion of Humphrey merely discloses that various processors (i.e., presumably the microprocessors illustrated in Fig. 1), may be selectively connected to first and second memory banks. This portion of Humphrey has nothing to do with receiving data frame information from any group of receive devices, much less a first group of receive devices and a second group of receive devices. This portion of Humphrey also does not disclose or suggest that when data frame information from a second group of receive devices is being transferred to one of the first and second memories, data frame information from a first group of receive devices is being transferred to the other of the first and second memories, as further required by claim 10.

Humphrey at col. 5, lines 44-63 discloses that each memory cycle has two phases. During the first phase, the enabled processor puts identical addresses on both the A and B common buses 102 and 104 while 16-bit processors access only their dedicated common bus. During the second phase, data from the addressed memory cell is read on either the A read bus, B read bus or concurrently on both the A and B buses. In the event of a write cycle, the write data is placed on the respective common bus (Humphrey – col. 4, lines 44-54 and Fig. 1). This portion of Humphrey further discloses that both processors 114 and 116, or processors 116 and 118, might operate concurrently during a given memory cycle over their respective A and B buses. To accomplish this, node control 130 places the processor slot ID code associated with

processor 114 on the A section of the slot processor ID bus and places the processor ID code associated with processor 116 on the B portion of the slot processor bus (Humphrey – col. 5, lines 55-63).

These portions of Humphrey do not disclose or suggest alternating the transferring of data frame information from a first group of the receive devices to the first and second memories, and alternating the transferring of data frame information from a second group of the receive devices to the first and second memories, much less that when data frame information from the second group of receive devices is being transferred to one of the first and second memories, data frame information from the first group of receive devices is being transferred to the other of the first and second memories, as recited in claim 10. In contrast, these portions of Humphrey merely disclose a method in which one of processors 110-118 accesses one of buses 102-108 during a read or write cycle. Humphrey clearly does not disclose alternating the transferring of data frame information from a first group of receive devices to first and second memories or alternating the transferring of data frame information from a second group of receive devices to the first and second memories, as recited in amended claim 10.

Humphrey at col. 7, lines 58-61 discloses a fixed rotational assignment of times lots to each of the processors, as illustrated in Table II. This portion of Humphrey does not disclose or suggest alternating the transfer of data frame information from a first group of receive devices and alternating the transfer of data frame information from a second group of receive devices, as required by claim 10, much less that when data frame information from the second group of receive devices is being transferred to one of the first and second memories, data frame information from the first group of receive devices is being transferred to the other of the first

and second memories, as recited in claim 10.

Humphrey at col. 8, lines 25-62 discloses a channel bandwidth allocation scheme. In particular, this portion of Humphrey discloses:

> Each time-slot corresponds to one central memory cycle time, which is nominally 80 nanoseconds. Thus, the total time for the entire 16 time slots is 1.28 microseconds. This means that each time a processor gains access to one of the 16-bit buses A or B in a given time slot, it provides a channel data rate of 25 megabits per second. The aggregate data rate for all 16 time slots and both A and B buses is 400 megabits per second. In this hypothetical example, processor 1, a 32-bit processor, is shown as connected to both bus A and bus B and is granted access in time slots 1 and 5, thus providing a total channel bandwidth of 100 megabits per second. It should be noted that for 32-bit processors, the lower 16 bits of data are always connected to Memory Bank 0 and the upper 16 bits of data are always connected to Bank 1. Processor 2 is assumed to be a 16-bit processor and is connected only to bus A and is granted time slots 3 and 7, providing a 50 megabit data rate. Processor 3 is illustrated as a 16-bit processor and is connected only to bus B. It is allocated time slots 3 to communicate with Bank 0 and time slot 7 to communicate with Bank 1. Memory Banks 0 and 1 are switched between buses A and B by the aforementioned Bus/Bank select switch 138. Processor 4 is shown as a 16-bit processor arbitrarily connected only to bus A. It, along with processor 3, is allocated time slots 2, 4, 6 and 8, each processor accessing a different bank, i.e., processor 4 to Bank 0 during slot 2 and 6 and to Bank 1 during slots 4 and 8. In this way, memory exchanges between the Central Memory 100 and processors 4 and 5 can be interleaved, with each processor granted a 100 megabit per second bandwidth. One restriction which must be observed is that each 16-bit processor must be given at least two time slots, one in which to access Bank 0 and one in which to access Bank 1. A 32-bit processor, since it simultaneously accesses both banks, may be allocated as little as one time slot.

This portion of Humphrey has nothing to do with alternating the transferring of data frame information from a first group of receive devices to first and second memories or alternating the transferring data frame information from a second group of receive devices to the first and second memories, much less that when data frame information from the second group of receive devices is being transferred to one of the first and second memories, data frame information from the first group of receive devices is being transferred to the other of the first

and second memories, as recited in claim 10. In contrast, this portion of Humphrey merely discloses that a number of processors may be assigned time slots in an arbitration cycle, but does not disclose or suggest that any of the processors access the same first and second memories in an alternating manner as recited in claim 10.

In particular, Humphrey at col. 8, lines 49-55 discloses that "Processor 4 is shown as a 16-bit processor arbitrarily connected only to bus A. It, along with processor 3, is allocated time slots 2, 4, 6 and 8, each processor accessing a different bank, i.e., processor 4 to Bank 0 during slot 2 and 6 and to Bank 1 during slots 4 and 8. In this way, memory exchanges between the Central Memory 100 and processors 4 and 5 can be interleaved." As best understood by Appellants, this portion of Humphrey in conjunction with Table II at col. 8, lines 15-25 of Humphrey discloses that accesses to memory 100 may be interleaved during a channel bandwidth allocation cycle. This portion of Humphrey, however, does not disclose or suggest that any of the processors in Humphrey receive data frame information and alternate the transfer of data frame information from a first group of receive devices to first and second memories or alternate the transfer of data frame information from a second group of receive devices to the first and second memories, much less that when data frame information from the second group of receive devices is being transferred to one of the first and second memories, data frame information from the first group of receive devices is being transferred to the other of the first and second memories, as required by amended claim 10. In contrast, this portion of Humphrey merely discloses that particular processors may receive access to memory 100 during particular slots. Nowhere in this portion of Humphrey, or elsewhere, does Humphrey disclose or suggest transferring data from a first group of receive devices to first and second memories in an

alternating manner or transferring data from a second group of receive devices to first and second memories in an alternating manner, as recited in claim 10.

For at least these reasons, Humphrey does not disclose or suggest each of the features of claim 10. Accordingly, Appellants respectfully submits that the rejection of claims 10, 13, 15 and 22 is improper and reversal of the rejection is respectfully requested.

2. Claim 11

Claim 11 recites simultaneously transmitting selection signals to first and second receive devices for selectively outputting data stored in the first and second receive devices. The Office Action states that Humphrey discloses this feature and points to col. 5, lines 25-34 for support (Office Action – page 3). Appellants respectfully disagree.

Humphrey at col. 5, lines 25-34 discloses that node control logic 130 broadcasts the processor slot ID number of the processor designated to have access to either the A or B bus via bus 132. Humphrey further discloses that when the processor slot ID codes broadcasted on bus 132 match a given processor ID code and address bit 01 corresponds to the state of the bank/bus select line 138, that processor may execute a memory transfer operation (Humphrey – col. 5, lines 39-43). These portions of Humphrey do not disclose or suggest simultaneously transmitting selection signals to first and second receive devices for selectively outputting data stored in the first and second receive devices. In contrast, this portion of Humphrey merely discloses broadcasting processor slot ID numbers on a bus.

For at least these reasons, Humphrey does not disclose or suggest each of the features of claim 11. Accordingly, Appellants respectfully submits that the rejection of claim 11 is improper

and reversal of the rejection is respectfully requested.

B. Rejection under 35 U.S.C. § 103 based on Humphrey in view of Mann

In rejecting a claim under 35 U.S.C. § 103, the Examiner must provide a factual basis to support the conclusion of obviousness. In re Warner, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). Based upon the objective evidence of record, the Examiner is required to make the factual inquiries mandated by Graham v. John Deere Co., 86 S.Ct. 684, 383 U.S. 1, 148 USPQ 459 (1966). The Examiner is also required to explain how and why one having ordinary skill in the art would have been realistically motivated to modify an applied reference and/or combine applied references to arrive at the claimed invention. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

In establishing the requisite motivation, it has been consistently held that the requisite motivation to support the conclusion of obviousness is not an abstract concept, but must stem from the prior art as a whole to impel one having ordinary skill in the art to modify a reference or to combine references with a reasonable expectation of successfully achieving some particular realistic objective. See, for example, Interconnect Planning Corp. v. Feil, 227 USPQ 543 (Fed. Cir. 1985). Consistent legal precedent admonishes against the indiscriminate combination of prior art references. Carella v. Starlight Archery, 804 F.2d 135, 231 USPQ 644 (Fed. Cir. 1986); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985).

1. Claims 1 and 9

With these principles in mind, claim 1 recites a network device that includes a plurality of receive devices corresponding to ports on the network device, the receive devices configured to receive data frames from the stations. The Office Action states that Humphrey discloses these features and points to col. 1, lines 42-48 and Fig. 1, elements 114 and 116 for support (Office Action – page 5). Appellants respectfully disagree.

Humphrey at col. 1, lines 42-48 discloses that a data stream received from a host is divided into a sequence of blocks and includes a header and trailer. Elements 114 and 116 in Fig. 1 of Humphrey correspond to two 16 bit microcontrollers. These portions of Humphrey do not disclose or suggest a plurality of receive devices that correspond to ports on a network device, as required by claim 1. In contrast, the mciroprocessors of Humphrey are not at all related to ports on the network adapter of Humphrey.

Claim 1 also recites that the network device includes an external memory interface configured to: receive data from the plurality of receive devices, transfer a portion of the data received from a first group of the receive devices to a first memory and a second memory in an alternating manner, and transfer a portion of the data received from a second group of the receive devices to the first memory and the second memory in an alternating manner. The Office Action states that Humphrey discloses these features and points to col. 3, lines 1-16, col. 5, lines 55-63, col. 7, lines 58-61 and col. 8, lines 57-62 for support (Office Action – page 5). Appellants respectfully disagree.

As discussed above with respect to claim 10, these portions of Humphrey merely disclose a method in which one of processors 110-118 accesses one of buses 102-108 during a read or

write cycle. None of the cited portions of Humphrey discloses or suggests transferring a portion of the data received from a first group of the receive devices to a first memory and a second memory in an alternating manner, and transferring a portion of the data received from a second group of the receive devices to the first memory and the second memory in an alternating manner, as recited in claim 1.

Claim 1 further recites that the external memory interface is configured to generate odd address information when transferring data via a first external memory bus to the first memory, and generate even address information when transferring data via a second external memory bus to the second memory. The Office Action admits that Humphrey does not disclose this feature, but states that Mann discloses this feature and points to Mann at col. 2, lines 38-44 and col. 5, line 61 to col. 6, line 17 for support (Office Action – page 6). Mann, however, does not remedy the deficiencies in the disclosure of Humphrey discussed above.

For at least these reasons, the combination of Humphrey and Mann does not disclose or suggest each of the features of claim 1.

In addition, even if, for the sake of argument, the combination of Humphrey and Mann could be fairly construed to disclose or suggest each of the features of claim 1, the Office Action does not provide the requisite motivation under 35 U.S.C. § 103 as to why it would have been obvious to combine Humphrey and Mann.

For example, the Office Action states that it would have been obvious to use Mann's teaching in Humphrey's system "in order to allow fixed bus length systems work store information double that fixed bus length using dual memories" and points to col. 1, lines 56-65 of Mann for support (Office Action – page 6). This alleged motivation for combining Humphrey

and Mann is merely a conclusory statement regarding an alleged benefit of the combination. Such motivation does not satisfy the requirements of 35 U.S.C. § 103.

In addition, the portion of Mann relied upon as providing the motivation for combining these references (i.e., col. 1, lines 56-65) merely discloses that a conventional practice in the design of memory modules is to provide a module suitable for use with only one system bus or memory bus configuration. This general statement in Mann cannot be fairly construed as providing objective motivation for combining portions of Mann with Humphrey.

Appellants further assert that Humphrey is directed to a network communication adapter (Humphrey – Abstract) and Mann is directed toward a multiple mode memory module (Mann – Abstract). These two references are unrelated, other than the fact that both include memory devices, and are clearly directed to totally different areas of technology. The mere fact that one reference allegedly provides a missing teaching with respect to a claim does not provide objective motivation as to why it would have been obvious to combine otherwise unrelated references.

For at least these reasons, Appellants respectfully submit that the rejection of claim 1 is improper. Accordingly, reversal of the rejection of claims 1 and 9 is respectfully requested.

2. Claims 2 and 3

Claim 2 recites that the external memory interface includes a scheduler coupled to the receive devices and configured to enable the received data frames to be output to the first and second memories, the scheduler simultaneously outputting first and second selection signals for outputting data from one of the first group of receive devices and one of the second group of

receive devices, respectively. The Office Action states that Humphrey discloses this feature and points to col. 5, lines 25-34 for support (Office Action – page 6). Appellants respectfully disagree.

Humphrey at col. 5, lines 25-34 discloses that node control logic 130 broadcasts the processor slot ID number of the processor designated to have access to either the A or B bus via bus 132. Humphrey further discloses that when the processor slot ID codes broadcasted on bus 132 match a given processor ID code and address bit 01 corresponds to the state of the bank/bus select line 138, that processor may execute a memory transfer operation (Humphrey – col. 5, lines 39-43). These portions of Humphrey do not disclose or suggest that node control logic 130 simultaneously transmits selection signals for outputting data from one of the first group of receive devices and one of the second group of receive devices, as recited in claim 2. In contrast, this portion of Humphrey merely discloses broadcasting processor slot ID numbers on a bus. Mann also does not disclose or suggest this feature.

For at least these reasons, Appellants respectfully submits that the rejection of claim 2 is improper. Accordingly, reversal of the rejection of claims 2 and 3 is respectfully requested.

3. Claims 4 and 5

Claim 4 recites that the external memory interface is further configured to simultaneously transfer the portions of the data from the first and second groups of receive devices to the first and second memories. The Office Action states that Humphrey discloses this feature and points to col. 5, lines 9-13 and lines 25-34 for support (Office Action – page 6). Appellants respectfully disagree.

Humphrey at col. 5, lines 9-13 discloses that processors 110 and 112 communicate with central memory 100 in a 32-bit mode by virtue of being concurrently connected to both the A and B buses and each 32-bit transfer generally involves 16 bits from Bank 0 and 16 bits from Bank 1. This portion of Humphrey apparently discloses transferring data to a central memory 100 by transferring data from two data banks (Bank 0 and Bank 1). This portion of Humphrey does not disclose or suggest transferring portions of the data from first and second groups of receive devices to the first and second memories, as required by claim 4.

Humphrey at col. 5, lines 25-35 discloses that node control logic 130 broadcasts processor slot ID numbers on bus 132. This portion of Humphrey also does not disclose or suggest an external memory interface that is further configured to simultaneously transfer the portions of the data from the first and second groups of receive devices to the first and second memories, as required by claim 4.

For at least these reasons, Appellants respectfully submit that the rejection of claim 4 is improper. Accordingly, reversal of the rejection of claims 4 and 5 is respectfully requested.

4. Claim 12

Claim 12 is dependent on claim 10 and is believed to be allowable for at least the reasons claim 10 is allowable. Mann does not remedy the deficiencies in Humphrey discussed above with respect to claim 10. In addition, Appellants assert that it would not have been obvious to combine portions of Mann and Humphrey for the reasons discussed above with respect to claim 1.

For at least these reasons, Appellants respectfully submit that the rejection of claim 12 is

improper and reversal of the rejection of claim 12 is respectfully requested.

5. Claims 16 and 19

Claim 16 recites a data communication system for controlling the communication of data frames between stations, that includes a plurality of receive devices configured to receive data frames from the stations and a scheduler coupled to the plurality of receive devices and configured to generate selection signals to selectively output data frame information from the receive devices. The Office Action states that Humphrey discloses this feature and points to col. 5, lines 25-34 for support (Office Action – page 8). Appellants respectfully disagree.

Humphrey at col. 5, lines 25-34, as discussed above, discloses that node control logic 130 broadcasts the processor slot ID number of the processor designated to have access to either the A or B bus via bus 132. Humphrey further discloses that when the processor slot ID codes broadcasted on bus 132 match a given processor ID code and address bit 01 corresponds to the state of the bank/bus select line 138, that processor may execute a memory transfer operation (Humphrey – col. 5, lines 39-43). These portions of Humphrey do not disclose or suggest a scheduler coupled to a plurality of receive devices configured to receive data frames from the stations, as required by claim 16, much less that node control logic 130 generates selection signals to selectively output data frame information from the receive devices. In contrast, these portions of Humphrey disclose that node control logic 130 is coupled to a number of microprocessors (Humphrey – Fig. 1). Such microprocessors are not equivalent to receive devices that receive data frames from stations. In addition, node control logic 130 does not

generate the claimed selection signals to selectively output data frame information from the receive devices.

Claim 16 also recites that the data communication system includes a switching device configured to receive the data frame information and simultaneously transfer data frame information from one of a first group of receive devices via a first external memory bus and data frame information from one of a second group of receive devices via a second external memory bus. The Office Action states that Humphrey discloses these features and points to col. 3, lines 1-16, col. 5, lines 55-63, col. 7, lines 58-61 and col. 8, lines 57-62 for support (Office Action – page 8). Appellants respectfully disagree.

As discussed above, these portions of Humphrey merely disclose that a number of microprocessors may be assigned slots in an arbitration cycle. None of these portions of Humphrey discloses or suggests that any of the microprocessors in Humphrey transfer data frame information from a first group of receive devices to the first and second external memory buses in an alternating manner, as required by claim 16. Further, none of these portions of Humphrey discloses or suggest that any of the microprocessors in Humphrey transfers data frame information from a second group of receive devices to the first and second external memory buses in an alternating manner, as also required by claim 16. Mann also does not disclose or suggest these features.

Therefore, as a factual matter, the combination of Humphrey and Mann does not disclose or suggest each of the features of claim 16.

In addition, even if, for the sake of argument, the combination of Humphrey and Mann could be fairly construed to disclose or suggest each of the features of claim 16, Appellants assert

that the motivation to combine Humphrey and Mann does not satisfy the requirements of 35 U.S.C. § 103 for the reasons discussed above with respect to claim 1.

For at least these reasons, Appellants respectfully submit that the rejection of claim 16 is improper. Accordingly, reversal of the rejection of claims 16 and 19 is respectfully requested.

6. Claim 17

Claim 17 recites that the system includes first and second multiplexers coupled to the first and second groups of the receive devices, respectively, each of the first and second multiplexers being configured to receive the selection signals from the scheduler and to output a portion of a data frame. The Office Action states that Humphrey discloses these features and points to Fig. 6a, elements 402, 416 and 428 for support (Office Action – page 10). Appellants respectfully disagree.

Elements 402, 416 and 418 in Humphrey correspond to multiplexers that may be included within one of the 16-bit microcontrollers (Humphrey – col. 13, lines 27-30). More particularly, these multiplexers are controlled by sequence control 480 to control the movement of all data within the microprocessor (Humphrey – col. 19, lines 4-7). These multiplexers of Humphrey cannot be construed as being equivalent to the claimed first and second multiplexers that are coupled to the first and second groups of receive devices, much less that each of these multiplexers is configured to receive selection signals from the claimed scheduler and to output a portion of a data frame. In contrast, these multiplexers in Humphrey are merely multiplexers located internally within a single microprocessor.

For at least these reasons, Appellants respectfully submit that the rejection of claim 17 is improper. Accordingly, reversal of the rejection of claim 17 is respectfully requested.

7. Claim 18

Claim 18 recites that the switching device is further configured to transfer data received from the first multiplexer to the first and second external memory buses in an alternating manner and to transfer data received from the second multiplexer to the first and second external memory in an alternating manner. The Office Action states that Humphrey discloses this feature and points to col. 5, lines 9-13, 25-34 and 39-54 for support (Office Action – page 10). Appellants respectfully disagree.

As discussed above with respect to claim 17, Humphrey does not disclose or suggest the claimed first and second multiplexers. Therefore, Humphrey cannot further disclose or suggest a switching device that is configured to transfer data received from the first and second multiplexers. Further, even if, for the sake of argument, Humphrey could be construed as disclosing the claimed first and second multiplexers, Humphrey does not disclose or suggest a switching device that is configured to transfer data received from the first multiplexer to first and second external memory buses in an alternating manner and to transfer data received from the second multiplexer to the first and second external memory buses in an alternating manner, as required by claim 18.

Humphrey at col. 5, lines 9-13, 25-34 and 39-54 discloses that node control logic 130 broadcasts processor slot ID numbers on bus 132, which is accessible to a number of microprocessors. Appellants note that these portions of Humphrey do not disclose or suggest

transferring data received from any of multiplexers 402, 416 and 428 (alleged to be equivalent to the claimed first and second multiplexers), as required by claim 18, much less transferring data received from a first multiplexer to first and second memory buses in an alternating manner or transferring data received from a second multiplexer to first and second memory buses in an alternating manner, as required by claim 18.

For at least these reasons, Appellants respectfully submit that the rejection of claim 18 is improper. Accordingly, reversal of the rejection of claim 18 is respectfully requested.

8. Claims 21 and 23

Claim 21 recites that the external memory interface is further configured to transfer data from one of the first group of receive devices to the first memory during a first clock cycle, transfer data from one of the second group of receive devices to the second memory during the first clock, transfer data from one of the first group of receive devices to the second memory during a second clock cycle, the second clock cycle immediately succeeding the first clock cycle, and transfer data from one of the second group of receive devices to the first memory during the second clock cycle. The Office Action states that Humphrey discloses these features and points to col. 3, lines 1-16, col. 5, liens 55-63, col. 7, lines 58-61 and col. 8, lines 57-62 for support (Office Action – page 11). Appellants respectfully disagree.

The above-cited portions of Humphrey have been discussed above. None of these portions of Humphrey disclose or suggest transferring data from one of a first group of receive devices to the first memory and data from one of a second group of receive devices to a second memory during a first clock cycle and transferring data from one of the first group of receive

devices to the second memory and a data from one of the second group of receive devices to the first memory during a second clock cycle, as required by claim 21. In contrast, these portions of Humphrey disclose transferring data in and out of a central memory 100 via a number of microprocessors (Humphrey – col. 5, lines 25-52). These portions of Humphrey are not at all related to transferring data from first and second groups of receive devices in the manner recited in claim 21.

For at least these reasons, Appellants respectfully submit that the rejection of claim 21 is improper. Accordingly, reversal of the rejection of claims 21 and 23 is respectfully requested.

C. Rejection under 35 U.S.C. § 103 based on Humphrey in view of Mann and further in view of Runaldue

1. Claim 7

Claim 7 recites that the first and second external memory buses are each 8-bytes wide and operate at a frequency of 100 MHz. The Office Action admits that the combination of Humphrey and Mann does not disclose this feature and relies upon Runaldue for disclosing an external memory that can operate at 100 MHz (Office Action – page 12). The Office Action states that it would have been obvious "to use Mann's teaching in Humphrey's system in order to allow fixed bus length systems work store information double that fixed bus length using dual memories" and points to col. 1, lines 56-65 of Mann for support (Office Action – page 12). The Office Action further states that it would have been obvious to use Runaldue's teaching "that external memory can operate at 100 MHz and enable Humphrey's switch to interface with memory at that speed" (Office Action – page 13). Appellants respectfully disagree.

Even if, for the sake argument, the combination of Humphrey, Mann and Runaldue could reasonably be construed to disclose each of the features of claim 7, the Office Action does not provide the requisite motivation under 35 U.S.C. § 103 as to why it would have been obvious to combine these references. That is, the alleged motivation statements for combining portions of Mann and Runaldue with Humphrey are merely conclusory statements regarding alleged benefits of the combination. Such motivation does not satisfy the requirements of 35 U.S.C. § 103 as to why it would have been obvious to combine these three disparate references.

For at least these reasons, Appellants respectfully submit that the rejection of claim 7 is improper. Accordingly, reversal of the rejection of claim 7 is respectfully requested.

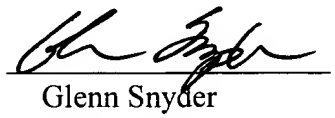
VIII. CONCLUSION

In view of the foregoing arguments, Appellants respectfully solicit the Honorable Board to reverse the Examiner's rejections of claims 1-5, 7, 9-13, 15-19 and 21-23.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

By: 
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IX. APPENDIX

1. A network device configured to control communication of data frames between stations, comprising:

a plurality of receive devices corresponding to ports on the network device, the receive devices configured to receive data frames from the stations; and

an external memory interface configured to:

receive data from the plurality of receive devices,

transfer a portion of the data received from a first group of the receive devices to a first memory and a second memory in an alternating manner, and

transfer a portion of the data received from a second group of the receive devices to the first memory and the second memory in an alternating manner,

generate odd address information when transferring data via a first external memory bus to the first memory, and

generate even address information when transferring data via a second external memory bus to the second memory.

2. The network device of claim 1, wherein the external memory interface includes:

a scheduler coupled to the receive devices and configured to enable the received data frames to be output to the first and second memories, the scheduler simultaneously outputting first and second selection signals for outputting data from one of the first group of receive devices and one of the second group of receive devices, respectively.

3. The network device of claim 2, wherein the external memory interface is further configured to simultaneously transfer 8 bytes of data from one of the first group of receive devices to the first memory and 8 bytes of data from one of the second group of receive devices to the second memory.

4. The network device of claim 1, wherein the external memory interface is further configured to simultaneously transfer the portions of the data from the first and second groups of receive devices to the first and second memories.

5. The network device of claim 1, wherein the external memory interface is configured to simultaneously transfer data received from a first one of the first group of the receive devices via the first external memory bus and a second one of the second group of the receive devices via the second external memory bus.

7. The network device of claim 5, wherein the first and second external memory buses are each 8-bytes wide and operate at a frequency of 100 MHz.

9. The network device of claim 1, wherein the external memory interface is further configured to simultaneously retrieve data from the first and second memories.

10. In a network device that controls communication of data frames between stations, a method of storing data frame information, comprising:

receiving a plurality of data frames;

temporarily storing the received data frames in a plurality of receive devices; and

simultaneously transferring data frame information to at least a first memory and a second memory, wherein the simultaneously transferring includes:

alternating the transferring of data frame information from a first group of the receive devices to the first and second memories, and

alternating the transferring of data frame information from a second group of the receive devices to the first and second memories, wherein when data frame information from the second group of receive devices is being transferred to one of the first and second memories, data frame information from the first group of receive devices is being transferred to the other of the first and second memories.

11. The method of claim 10, further comprising:

simultaneously transmitting selection signals to first and second receive devices for selectively outputting data stored in the first and second receive devices.

12. The method of claim 10, wherein the simultaneously transferring further includes:

transferring 8 bytes of data from a first receive device to the first memory and 8 bytes of data from a second receive device to the second memory.

13. The method of claim 10, wherein the simultaneously transferring further includes:

sending a portion of a first data frame via a first external memory bus and sending a portion of a second data frame via a second external memory bus.

15. The method of claim 10, further comprising:

simultaneously retrieving data frame information from the first and second memories.

16. A data communication system for controlling the communication of data frames between stations, comprising:

a plurality of receive devices configured to receive data frames from the stations;

a scheduler coupled to the plurality of receive devices and configured to generate selection signals to selectively output data frame information from the receive devices;

a switching device configured to:

receive the data frame information, and

simultaneously transfer data frame information from one of a first group of receive devices via a first external memory bus and data frame information from one of a second group of receive devices via a second external memory bus;

a first memory configured to receive data frame information from the first external memory bus; and

a second memory configured to receive data frame information from the second external memory bus, wherein the switching device is further configured to:

generate data address information having odd addresses for data transferred to the first memory,

generate data address information having even addresses for data transferred to the second memory,

transfer data frame information from the first group of receive devices to the first and second external memory buses in an alternating manner, and

transfer data frame information from the second group of receive devices to the first and second external memory buses in an alternating manner.

17. The system of claim 16, further comprising:

first and second multiplexers coupled to the first and second groups of the receive devices, respectively, each of the first and second multiplexers being configured to receive the selection signals from the scheduler and to output a portion of a data frame.

18. The system of claim 17, wherein the switching device is further configured to transfer data received from the first multiplexer to the first and second external memory buses in an alternating manner and to transfer data received from the second multiplexer to the first and second external memory buses in an alternating manner.

19. The system of claim 16, wherein the first memory is configured to store data words having odd addresses and the second memory is configured to store data words having even addresses.

21. The network device of claim 1, wherein the external memory interface is further

configured to:

transfer data from one of the first group of receive devices to the first memory during a first clock cycle,

transfer data from one of the second group of receive devices to the second memory during the first clock,

transfer data from one of the first group of receive devices to the second memory during a second clock cycle, the second clock cycle immediately succeeding the first clock cycle, and

transfer data from one of the second group of receive devices to the first memory during the second clock cycle.

22. The method of claim 10, wherein the alternating of the transferring of data frame information from the first group of receive devices to the first and second memories is performed each clock cycle.

23. The system of claim 16, wherein the switching device is further configured to:

alternate the transfer of data frame information from the first group of receive devices to the first and second external memory buses each clock cycle, and

alternate the transfer of data frame information from the second group of receive devices to the first and second external memory buses each clock cycle.

X. EVIDENCE APPENDIX

None

XI. RELATED PROCEEDINGS APPENDIX

None